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Remarks

Claims 1-7, 10-12, 14-15, and 24-28 are pending in this application. By the foregoing amendment, Applicant seeks to cancel claim 8-9,13, and 16, amend claims 1, 5-7, 10-12, 14-15, and add new claims 24-28. Claims 17-23 have been removed from consideration in response to a restriction requirement without prejudice or disclaimer. Applicant has provided a new abstract, and has amended the specification to correct informalities. These changes are believed to be fully supported by the specification and are not believed to introduce new matter. Thus, it is respectfully requested that the amendments and additions be entered by the Examiner. Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding rejections, and that they be withdrawn.

Rejections under 35 U.S.C. § 112

At paragraphs 5-6, claims 1-16 were rejected under 35 U.S.C. § 112, ¶ 2 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Based on the following remarks and amendments discussed below, the Applicant respectfully traverses this rejection.

Claim 1 recites a plurality of parallel tracks in a spiral pattern, each track having a first end and a second end, and having the first ends coupled together and the second ends coupled together. FIG. 28A illustrates one embodiment of the invention, where the first ends are coupled together at 2814, and the second ends are coupled together at 2810. FIG. 28C illustrates another embodiment having ends coupled together. Applicant asserts that claim 1 is definite in light of the plain meaning of the claim language ("first ends coupled together and the second ends coupled together") and the mentioned figures. Applicant also asserts that claim 1 is not limited to the embodiments of FIG. 28A and 28C.

Claim 2 recites that the substrate in FIG. 1 "is fabricated using a CMOS process". CMOS is an acronym for Complementary Metal Oxide Semiconductor, which is a well known semiconductor process to those skilled in the electrical arts, as is noted in the Office Action at paragraph 8. Applicant asserts that the recited "substrate" provides sufficient

structure for 35 U.S.C. § 112, ¶ 2 and that claim 2 simply recites the feature that the substrate of claim 1 can be fabricated using a CMOS process. Accordingly, Applicant asserts that claim 2 is sufficiently definite to meet the requirements of 35 U.S.C. § 112, ¶ 2.

Claims 8-9 have been canceled, as the diffusion layer recitation has been added to claim 1.

Claim 10 has been amended to recite that the fingered pattern is formed from n+ material having n+ fingers electrically isolated by polysilicon regions. FIG. 28E illustrates one embodiment of claim 10, where n+ regions 2866 are separated by polysilicon regions 2868. Therefore, Applicant asserts that claim 10 is sufficiently definite to meet the requirements of 35 U.S.C. § 112, ¶ 2.

Claim 11 has been amended so that it depends from claim 10, instead of claim 8. Claim 10 provides sufficient antecedent basis for the "fingered pattern" in claim 11. The term "a common ground reference" is well known to those skilled in the electrical arts, and therefore requires no further explanation. Accordingly, Applicant asserts that claim 11 is sufficiently definite to meet the requirements of 35 U.S.C. § 112, ¶ 2.

Claim 12 has been amended so that it depends from claim 11 instead of claim 8, so as to provide antecedent basis for "the common ground reference." The term "second fingered pattern" is used for the first time in claim 12, and therefore does not require antecedent basis support. Furthermore, the term "second fingered pattern" is properly introduced using "a", and not "the" or "said", since it is being introduced for the first time. Therefore, the "second fingered pattern" does not require any antecedent basis in claim 12.

Regarding claims 13-16, MPEP 2173.05(b) addresses the use of the term "substantially" in a claim, and reports that the Federal Circuit and the CCPA have found the this term to be definite. (MPEP 2173.05(b), *citing*, *In re Mattison*, 509.F2d. 563, 184 USPQ 484 (CCPA 1975), *also citing*, *Andrew Corp. vs Gabriel Electronics*, 847 F.2d 819, 6 USPQ 2d 2010 (Fed Cir., 1988). It is noted that in *In re Mattison*, the Federal Circuit found "substantially equal" to be definite, which is similar to the term "substantially identical" that is used in claims 13-14. Accordingly, Applicant asserts that claims 13-16, as filed, are sufficiently definite to meet the requirements of 35 U.S.C. § 112, ¶ 2. However, in order to

expedite prosecution, Applicant has canceled claim 13 and 16. Claims 14-15 have been amended to remove "substantially", in addition to other claim amendments.

Based on the discussion above, Applicant asserts that claim 1-7, 10-12, and 14-15 meet the requirements of 35 U.S.C. § 112, ¶ 2, and therefore request that these rejections be withdrawn.

Rejections under 35 U.S.C. § 103

At paragraphs 7-8, claims 1-3 and 5-14 and 16 were rejected under 35 U.S.C. § 103 as allegedly being obvious over U.S. Patent No. 5,852,866 to Kuettner *et. al.* (hereinafter "Kuettner"), in view of U.S. Patent No. 5,852,866 to Nasserbakht (hereinafter "Nasserbakht"), and further in view of U.S. Patent No. 5,966,063 to Sato *et. al.* (hereinafter "Sato"). Applicant respectfully traverses this rejection based on the arguments below.

Claim 1 has been amended to add the n+ diffusion layer recited in claim 9 so that the n+ diffusion layer is disposed in the substrate beneath the spiral inductor metalization pattern. The Office Action relies on Nasserbakht to teach a N^+ diffusion layer disposed beneath the spiral inductor metalization. Applicant disagrees with this interpretation. FIG. 3 of Nasserbakht illustrates that the P^+ diffusion region 40 and the N^+ diffusion region 42 are disposed on either side of the spiral trace 32, but not underneath the spiral trace 32 as is recited in Applicant's claim1. The P^+ diffusion region 40 and the N^+ diffusion region 42 are meant to form contacts 44 and 46 in FIG. 3, and not to provide a shield beneath the spiral 32. (*See,* Nasserbakht, FIG. 3, col.2, lines 37-40). Therefore, Nasserbakht does not teach the N^+ diffusion layer that is recited in Applicant's amended claim 1. Neither Kuettner or Sato cure this defect. As a result, the cited references do not teach or suggest each and every feature of Applicant's claim 1. Accordingly, Applicant requests that 35 U.S.C. § 103 rejection be removed, and that claim 1 and the respective dependant claims 2-7 and 10-12 be passed to allowance.

Additionally, regarding dependent claim 10, it is noted that the cited art does not teach the n^+ diffusion layer formed in *a fingered pattern* from n+ material having n+ fingers electrically isolated by regions of polysilicon to produce the fingered pattern. The recited

fingered pattern provides the desired shielding, but without undesirable eddy currents. (*See*, specification, page 76, lines 27-31, FIG. 28E)

New claim 24 recites a first and second spiral patterns that are on separate layers. The first spiral pattern has a first end and a second end, and the second spiral pattern also has a first end and a second end. The first end of the first spiral pattern is connected to the first end of the second spiral pattern to form an input for the spiral inductor. The second end of the first spiral pattern is connected to the second end of the second spiral pattern to form an output of the integrated circuit inductor.

The Office Action relies on Kuettner to teach multiple spirals on separate layers. Referring to FIG. 4 of Kuettner, double coil 21 on a first layer is connected to double coil 22 on a second layer by plated throughhole 25. The coils 21 and 22 are actually a single pair of coils that begin on one layer at contacts 24 and continue to the second layer through the plated throughhole 25 to end at contacts 23. As such, the contacts 24 on the first layer form an input for the coils 21 and 22, and the contacts 23 on the second layer form an output for the coils 21 and 22.

In contrast, Applicant's claim 24 recites first and second spirals on separate layers, where each spiral has *a first end and a second end* (i.e. input and output) on its respective layer. The first ends (on separate layers) are connected together to form an input, and the second ends are connected together (on the separate layers) to form an output. Kuettner cannot connect the contacts 23 and 24 together, because to do so would short the input directly to the output, which would short-out the coil inductance. Therefore, Kuettner does not teach or suggest connecting together a first end on one layer to a first end on a second layer to form an input, and also does not teach or suggest connecting together a second end on one layer to a second end on a second layer to form an output. Neither Nasserbakht or Sato cure this defect. As a result, the cited references do not teach or suggest each and every feature of Applicant's claim 24, and therefore these new claims 24-28 should be passed to allowance. Claim 15 is allowable for at least the same reasons as new claim 24 because it also includes the first ends on separate layer connected together to form an input, and second ends connected together to form an output.

Claim 14 recites a first track disposed on the first layer in a first spiral pattern, a second track disposed on the second layer in a second spiral pattern, and *a pattern of via holes sufficient to couple a varying voltage present along the length of the first track on to the second track.* As discussed above, FIG. 4 of Kuettner teaches double coil 21 on a first layer that is connected to double coil 22 on a second layer by plated throughhole 25. However, plated thoughhole 25 is only at a single location, and therefore is not capable of coupling a varying voltage present along *the length* of the coil 21 and 22, as recited by Applicant's claim 14. Furthermore, it would not be obvious to extend the plated throughole 25 to a pattern of via holes, because to do so would short coil 21 to coil 22, and therefore short the input contact 24 to the output contact 23, thereby eliminating the desired inductance. In sum, *the pattern of vias holes* recited in claim 14 is not taught or suggested by Kuettner or the other cited references. Therefore, Applicant requests that 35 U.S.C. § 103 rejection be removed, and that claim 14 be pass to allowance.

For at least the reasons discussed above, Applicant asserts that independent claims 1, 14, 15, and 24, and their respective dependant claims are allowable over the cited references. Accordingly, Applicant requests that these claims be passed to allowance.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeffrey Helvey
Attorney for Applicants
Registration No. 44,757

Date: 3/13/02

1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934
(202) 371-2600

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Version with markings to show changes made

In the Abstract:

A new abstract has been provided.

In the Specification:

On page1, please amend the paragraph starting on line 10, as follows:

This application is a continuation-in-part of patent application entitled "System and Method for ESD Protection," by Agnes N. Woo, Kenneth R. Kindsfater, and Fang Lu, filed January 14, 2000, U.S. Patent Application No. 09/483,551 [to be assigned (Docket B600:34208)]; which is a continuation-in-part of U.S. Patent Application No. 09/439,101 filed November 12, 1999; the disclosures of which are incorporated herein by reference.

On page 80, please amend the paragraph starting on line 15, as follows:

FIG. 32 shows a transconductance stage 3102 with an LC load 3104 that is provided with Q enhancement 3202 and Q compensation over temperature 3206. Q enhancement 3202 tends to increase the circuit Q thus, increasing the frequency selectivity of the circuit. A Q enhancement is provided by the transconductance element's G_m 3202 connected as shown. Addition of this transconductance element is equivalent to adding a negative resistance 3024 that is temperature dependent in parallel with R'(T). This negative resistance tends to cause cancellation of the parasitic resistance thus, tending to increase the circuit Q. The details of Q enhanced filters are disclosed in more detail in U.S. Patent Application No.09/573,356, filed 5/17/00 [_____filed _____(B600:_____)] entitled, "New CMOS Differential Pair Linearization Technique" by Haideh Khorramabadi; based on U.S. Provisional Application No. 60/136,115 filed May 26, 1999 (B600:34678), the subject matter of which is incorporated in this application in its entirety by reference. Once an improved Q is

achieved it is desirable to maintain it over the range of temperatures encountered in circuit operation with temperature compensation circuitry 3206.

On page 105, amend the paragraph starting on line 5 as follows:

A more detailed description of the VCO tuning scheme is provided in U.S. Patent Application No. [_____] 09/580,014, filed [_____] May 26,2000, (B600:36226) entitled "System and Method for Narrow Band PLL Tuning" by Ralph Duncan and Tom W. Kwan; based on U.S. Provisional Application No. 60/136,116 filed May 26, 1999 (B600:34677), the subject matter which is incorporated in its entirety by reference. Once the fine, or narrow band PLL has been tuned such that is has been locked its frequency may be used in conjunction with the frequency generated by the coarse PLL to provide channel tuning as previously described for the coarse/fine PLL tuning of FIGS. 21 and 22.

On page 144, amend the paragraph starting on line 12, as follows:

The details of ESD protection are disclosed in more detail in U.S. Patent Application No.09/483,551 [_____] filed January 14, 2000 [(B600:34208)] entitled "System and Method for ESD Protection" by Agnes N. Woo, Kenneth R. Kindsfater and Fang Lu based on U.S. Provisional Application No 60/116,003 filed January 15, 1999; U.S. Provisional Application No. 60/117,322 filed January 26, 1999; and U.S. Provisional Application No. 60/122,754 filed February 25, 1999; the subject matters of which are incorporated in this application in their entirety by reference.

In the Claims:

Please amend the following claims.

1. (Once Amended) An integrated circuit inductor comprising:

a substrate; [and]

a spiral inductor metalization pattern disposed on the substrate including a plurality of parallel tracks in a spiral pattern each track having a first end and a second end and having the first ends coupled together and the second ends coupled together; and

a n+ diffusion layer disposed in the substrate beneath the spiral inductor metalization pattern.

5. (Once Amended) The integrated circuit inductor of claim 1, in which the [multiple] plurality of tracks are disposed in a common layer of the substrate.

6. (Once Amended) The integrated circuit inductor of claim 1, in which the [multiple] plurality of tracks are disposed in different layers of the substrate.

7. (Once Amended) The integrated circuit inductor of claim 1, in which the [multiple tracks] plurality of tracks are disposed in different layers of the substrate and coupled together with a via.

10. (Once Amended) The integrated circuit inductor of claim [8]1, in which [the shield] the n^+ diffusion layer is formed in a fingered pattern from n+ material having n+ fingers electrically isolated by regions of polysilicon to produce the fingered pattern.

11.(Once Amended) The integrated circuit inductor of claim [8]10, in which the fingered pattern is coupled to a common ground reference.

12.(Once Amended) The integrated circuit inductor of claim [8]10, in which the [shield] n^+ diffusion layer further comprises a second fingered pattern coupled to the common ground reference by a conductive strip that does not provide a ground loop path.

14. (Once Amended) An integrated circuit inductor comprising:

a substrate having a first layer and a second layer;

a first track disposed on the first layer in a first spiral pattern;

a second track disposed on the second layer in a second spiral pattern [substantially identical to the first spiral patten] and [substantially] oriented parallel to the first spiral pattern; and

a pattern of via holes sufficient to couple a varying voltage present along the length of the first track on to the second track.

15. (Once Amended) An integrated [inductance] inductor comprising:

a substrate having a first layer and a second layer;

a first outer transmission line disposed on the first layer in a spiral pattern;

a second inner transmission line disposed on the first layer in a spiral pattern such that the second inner transmission line is loosely coupled to the first outer transmission line; [and having]

a first transmission line first end of the first outer transmission line directly coupled to a second transmission line first end of the second inner transmission line, and a first transmission line second end of the first outer transmission line directly coupled to a second transmission line second end of the second inner transmission line;

a third outer transmission line disposed on the second layer in a spiral pattern and aligned [substantially directly] above the first transmission line and directly coupled to the first transmission line; [and]

a fourth inner transmission line disposed on the substrate's second layer in a spiral pattern such that the fourth inner transmission line is coupled to the first transmission line and aligned [substantially directly] above the second transmission line and directly coupled to the second transmission line[.] ;and

the first transmission line first end and the second transmission line first end forming an input for the integrated inductor, the first transmission line second end and the second transmission line second end forming an output for the integrated inductor.

Claims 8-9, 13, and 16 have been canceled.

New claims 24-28 have been added.